

PATENT NUMBER

## U.S. UTILITY Patent Application

12W O.I.P.E. SCANNED <u>0m12</u> Q.A. <u>0m12</u>	PATENT DATE
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APPLICATION NO. 09/540591	CONT/PRIOR	CLASS <del>275</del> 370	SUBCLASS 503	ART UNIT <del>2704</del> 2665	EXAMINER <del>JIN6</del> KIM	HSU
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## APPLICANTS

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**TITLE**

Bus control module for a multi-stage clock distribution scheme in a signaling server

PTO-2040  
12/99

**ISSUING CLASSIFICATION**

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>		
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.	
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			<b>NOTICE OF ALLOWANCE MAILED</b>		
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____  _____  _____	_____ (Primary Examiner) (Date)			<b>ISSUE FEE</b>		
				Amount Due		Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)			<b>ISSUE BATCH NUMBER</b>		
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